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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,551	09/16/2003	William J. Borland	EL0496 US NA	2580

23906 7590 11/15/2005

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/663,551	BORLAND ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-12, and 14-23 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,144,526 (Vu).

Vu discloses, referring to figure 1, a printed wiring board comprising a first circuit conductor (9) extending through at least a part of the printed wiring board, a second circuit conductor (9) extending through at least a part of the printed wiring board, and a plurality of stacked innerlayer panels, wherein at least one of the innerlayer panels comprises at least one capacitor (see col. 2, lines 10-15), comprising a first electrode (3) formed from a foil and having a first electrode termination coupled to the first circuit conductor wherein the first electrode termination is within the footprint of the first electrode, at least one dielectric layer comprising a high dielectric constant material (5) disposed over the first electrode including an aperture formed therethrough, and a second electrode (3) formed over the first dielectric layer and having a second electrode termination coupled to the second circuit conductor, wherein the second electrode termination is spaced a selected distance from the first electrode termination to reduce separation between terminations [claim 1], wherein the first circuit conductor extends through the dielectric layer [claim 2], wherein the capacitor of the at least one innerlayer

panel is laminated to a laminate material (7) disposed over the capacitor, wherein the first circuit conductor extends through the laminate material (see figure 2) [claim 4], wherein the second circuit conductor extends through the laminate material (see figure 2) [claim 5]

Similarly, Vu discloses, referring to figure 2, a printed wiring board comprising a first circuit conductor (15) extending through at least a part of the printed wiring board, a second circuit conductor (15) extending through at least a part of the printed wiring board, and a plurality of stacked innerlayer panels, wherein at least one of the innerlayer panels comprises at least one capacitor (see col. 2, lines 10-15), comprising a first electrode (13) formed from a foil and having a first electrode termination coupled to the first circuit conductor wherein the first electrode termination is within the footprint of the first electrode, at least one dielectric layer comprising a high dielectric constant material (17) disposed over the first electrode including an aperture formed therethrough, and a second electrode (13) formed over the first dielectric layer and having a second electrode termination coupled to the second circuit conductor, wherein the second electrode termination is spaced a selected distance from the first electrode termination to reduce separation between terminations [claim 1], the capacitor further comprising a third electrode spaced from the second electrode by a two-layer dielectric (17, 19) and electrically connected to the first electrode [claim 6], wherein the first electrode has a first component side that contacts the dielectric layer and a second side opposite to the first component side wherein the first circuit conductor extends from the second side of the first electrode [claim 7], wherein the termination of the second

electrode is within the footprint of the second electrode [claim 8], further comprising a laminate material (7) disposed over the second side of the first electrode, wherein the first circuit conductor extends through the laminate material and the second circuit conductor extends through the laminate material [claim 9], the capacitor further comprising a third electrode spaced from the second electrode by a two-layer dielectric (17, 19) electrically connected to the first electrode [claim 10].

Additionally, Vu discloses, referring to figure 1, a method of making a printed writing board comprising, forming a plurality of stacked innerlayer panels, wherein forming at least one of the innerlayer panels comprises, providing a metallic foil (3), forming a dielectric layer (5) comprising a high dielectric constant material over the metallic foil and including an aperture formed therethrough, forming a first electrode from the metallic foil, the first electrode having a first electrode termination located within the footprint of the first electrode, and forming a second electrode (3) over the dielectric layer, the second electrode having a second electrode termination, wherein the first electrode, the second electrode, and the dielectric form a capacitor, and wherein the second electrode termination is spaced a selected distance from the first electrode termination to reduce separation between terminations, forming a first circuit conductor (9), wherein the first circuit conductor extends through at least a portion of the printed wiring board and contacts the first electrode termination, and forming a second circuit conductor (9), wherein the second circuit conductor contacts the second electrode termination and extends through at least a portion of the printed wiring board [claim 11], wherein the first circuit conductor extends through the aperture of the

dielectric layer [claim 12] wherein forming the innerlayer panel comprises forming a laminate material (7) over the first and second electrodes and over the dielectric [claim 14], wherein forming the first circuit conductor comprise forming a conductive via through the laminate material, and forming the second circuit conductor comprises forming a conductive via through the laminate material (see col. 2, lines 15-20) [claim 15].

In similar fashion, Vu discloses, referring to figure 2, a method of making a printed writing board comprising, forming a plurality of stacked innerlayer panels, wherein forming at least one of the innerlayer panels comprises, providing a metallic foil (13), forming a dielectric layer (17) comprising a high dielectric constant material over the metallic foil and including an aperture formed therethrough, forming a first electrode from the metallic foil, the first electrode having a first electrode termination located within the footprint of the first electrode, and forming a second electrode (13) over the dielectric layer, the second electrode having a second electrode termination, wherein the first electrode, the second electrode, and the dielectric form a capacitor, and wherein the second electrode termination is spaced a selected distance from the first electrode termination to reduce separation between terminations, forming a first circuit conductor (15), wherein the first circuit conductor extends through at least a portion of the printed wiring board and contacts the first electrode termination, and forming a second circuit conductor (15), wherein the second circuit conductor contacts the second electrode termination and extends through at least a portion of the printed wiring board [claim 11], wherein forming the innerlayer panel comprises forming a third electrode (13

spaced from the second electrode by a two-layer dielectric and electrically connected to the first electrode, wherein the first electrode, the second electrode, the third electrode and the dielectric layer form the capacitor [claim 16], wherein forming the innerlayer panel comprise, providing a laminate material, and laminating the metallic foil to the laminate material before forming the first electrode (see col. 2, lines 25-45) [claim 17], wherein the first electrode has a first component side that contacts the dielectric, and a second side opposite to the first side, wherein forming the first circuit conductor comprises forming the first circuit conductor to extend from the second side of the first electrode [claim 18], wherein the second electrode termination is within the footprint of the second electrode, and forming the innerlayer panel comprises forming a laminate material over the second side of the first electrode [claim 19], wherein forming a first circuit conductor comprise forming a conductive via through the laminate material, and forming a second circuit conductor comprises forming a conductive via through the laminate material (see col. 2, lines 15-20) [claim 20], wherein forming the innerlayer panel comprise, forming a third electrode spaced from the second electrode by a two-layer dielectric (17, 19) and electrically connected to the first electrode, wherein the first electrode, the second electrode, the third electrode and the dielectric from the capacitor [claim 21], wherein forming the innerlayer panel comprises, providing a laminate material and laminating the metallic foil to the laminate material before forming the first electrode (se col. 2, lines 20-45) [claim 22], wherein forming a plurality of stacked innerlayer panels comprises providing a specified number of innerlayer panels, joining the innerlayer panels together, forming a third circuit conductor through at least two of

the joined innerlayer panels and incorporating the joined innerlayer panels into the printed wiring board [claim 23].

Claims 1-3 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,274,224 (O'Bryan).

O'Bryan discloses, referring to figure 3B, a printed wiring board comprising a first circuit conductor (36b) extending through at least a part of the printed wiring board, a second circuit conductor (36b') extending through at least a part of the printed wiring board, and a plurality of stacked innerlayer panels, wherein at least one of the innerlayer panels comprises at least one capacitor (see col. 13, lines 10-15), comprising a first electrode (33b) formed from a foil and having a first electrode termination coupled to the first circuit conductor wherein the first electrode termination is within the footprint of the first electrode, at least one dielectric layer (34b) comprising a high dielectric constant material (see col. 2, lines 10-15) disposed over the first electrode including an aperture formed therethrough, and a second electrode (35b) formed over the first dielectric layer and having a second electrode termination coupled to the second circuit conductor, wherein the second electrode termination is spaced a selected distance from the first electrode termination to reduce separation between terminations [claim 1], wherein the first circuit conductor extends through the dielectric layer [claim 2], wherein the second electrode termination is within the footprint of the second electrode, and the second circuit conductor extends through the aperture of the dielectric layer [claim 3].

Similarly, O'Bryan discloses, referring to figure 3B, a method of making a printed writing board comprising, forming a plurality of stacked innerlayer panels, wherein forming at least one of the innerlayer panels comprises, providing a metallic foil (33b), forming a dielectric layer (34b) comprising a high dielectric constant material over the metallic foil and including an aperture formed therethrough, forming a first electrode from the metallic foil, the first electrode having a first electrode termination located within the footprint of the first electrode, and forming a second electrode (35b) over the dielectric layer, the second electrode having a second electrode termination, wherein the first electrode, the second electrode, and the dielectric form a capacitor, and wherein the second electrode termination is spaced a selected distance from the first electrode termination to reduce separation between terminations, forming a first circuit conductor (36b), wherein the first circuit conductor extends through at least a portion of the printed wiring board and contacts the first electrode termination, and forming a second circuit conductor (36b'), wherein the second circuit conductor contacts the second electrode termination and extends through at least a portion of the printed wiring board [claim 11], wherein the first circuit conductor extends through the aperture of the dielectric layer [claim 12], wherein the second electrode termination is within the footprint of the second electrode and forming the second circuit conductor comprises forming a conductive via that extends through the dielectric layer [claim 13].

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose PWBs with embedded capacitors:

US 5,099,388 Ogawa et al.,

US 5,378,662 Tsuyuki,

US 5,590,017 Kelso,

US 6,184,567 Fujisawa et al.,

US 6,201,684 Kobayashi et al..

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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SUPERVISORY PATENT EXAMINER
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